TOP ONE SEMI CONDUCTOR

NE555

GENERAL PURPOSE SINGLE BIPOLAR TIMERS

DESCRIPTION

The NE555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external re- sistor and capacitor. For a stable operation as an os- cillator, the free running frequency and the duty cy-cle are both accurately controlled with two external resistors and one capacitor. The circuit may be trig-gered and reset on falling waveforms, and the out-put structure can source or sink up to 200mA. The NE555 is available in plastic and ceramic minidip package and in a 8-lead micropackage and in metal can package version.

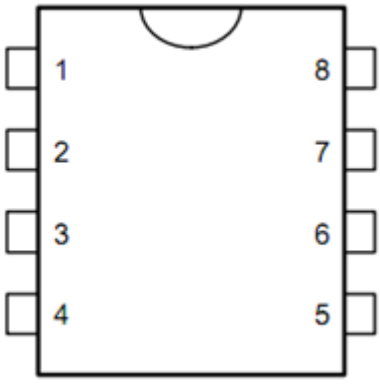
FEATURES

- Low turn off time
- Maximum operating frequency greater than 500khz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current can source or sink 200ma
- Adjustable duty cycle
- Ttl compatible
- Temperature stability of 0.005% peroc

N
DIP8
(Plastic Package)

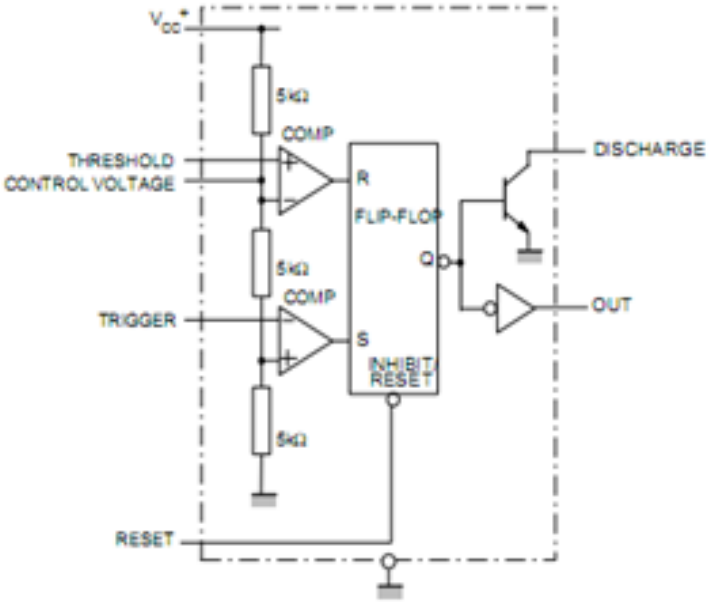
D
SO8
(Plastic Micropackage)

PIN CONNECTIONS (top view)

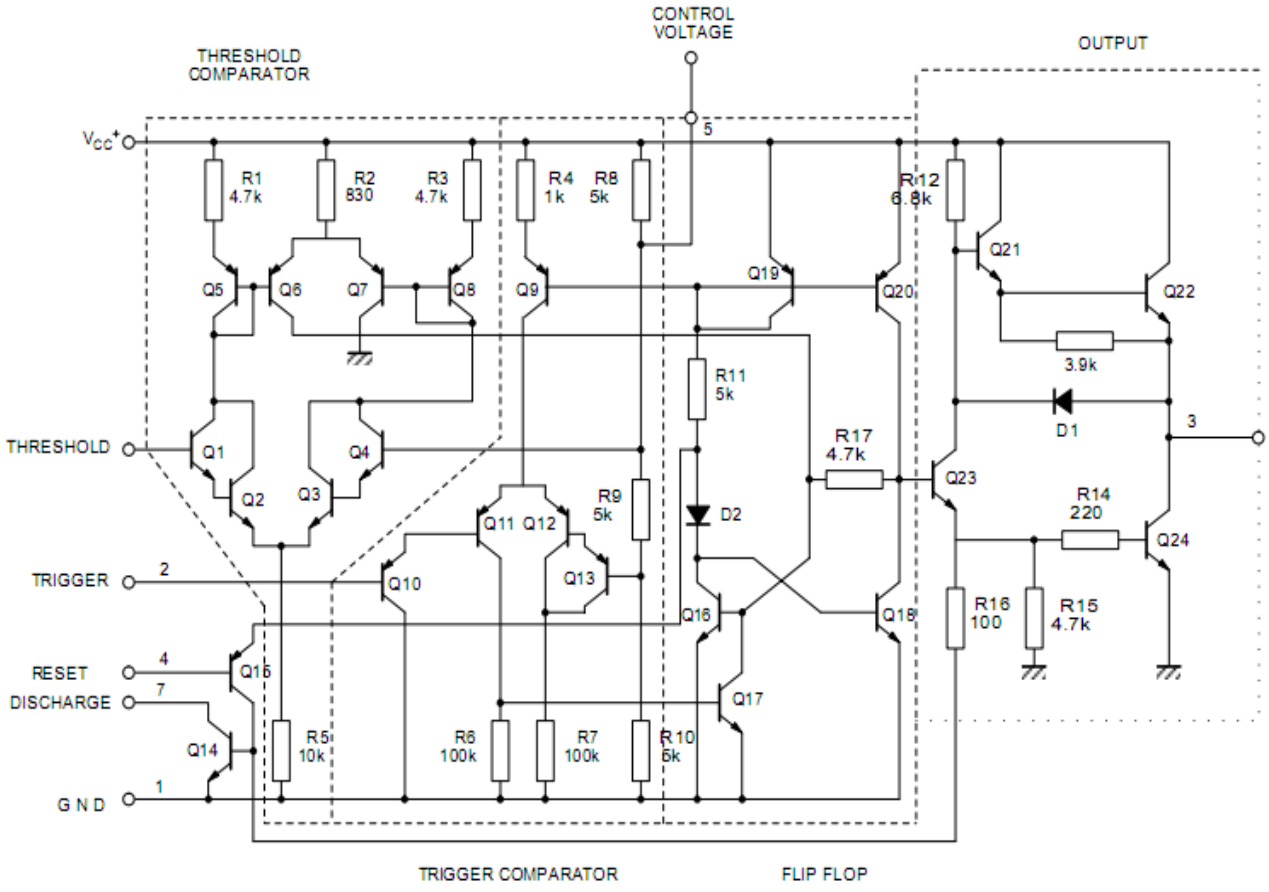


1 - GND
2 - Trigger
3 - Output
4 - Reset
5 - Control voltage
6 - Threshold
7 - Discharge
8 - Vcc

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{cc}	Supply Voltage	18	V
Toper	Operating Free Air Temperature Range for NE555	0 to 70	0C
T_j	Junction Temperature	150	^{0}C
T_{stg}	Storage Temperature Range	– 65 to 150	^{0}C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 18	V
V_{th}, V_{trig}, V_{cl}, V_{reset}	Maximum Input Voltage	V_{CC}	V

ELECTRICAL CHARACTERISTICS

T_{amb} = +25^{o}C, V_{CC} = +5V to +15V (unless otherwise specified

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
I_{CC}	Supply Current (RL ∞) (- note 1) Low State V_{CC} = +5V V_{CC} = +15V High State V_{CC} = 5V		 3 10 2	 6 15	mA
	Timing Error (monostable) (R_A = 2k to 100kΩ, C = 0.1μF) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 1 50 0.1	 3 0.5	% ppm/°C %/V
	Timing Error (astable) (R_A, R_B = 1kΩ to 100kΩ, C = 0.1μF, V_{CC} = +15V) Initial Accuracy - (note 2) Drift with Temperature Drift with Supply Voltage		 2.25 150 0.3		% ppm/°C %/V
V_{CL}	Control Voltage level V_{CC} = +15V V_{CC} = +5V	 9 2.6	 10 3.33	 11 4	V
V_{th}	Threshold Voltage V_{CC} = +15V V_{CC} = +5V	 8.8 2.4	 10 3.33	 11.2 4.2	V
I_{th}	Threshold Current - (note 3)		0.1	0.25	μA
V_{trig}	Trigger Voltage V_{CC} = +15V V_{CC} = +5V	 4.5 1.1	 5 1.67	 5.6 2.2	V
I_{trig}	Trigger Current (V_{trig} = 0V)		0.5	2.0	μA
V_{reset}	Reset Voltage	0.4	0.7	1	V

I_{reset}	Reset Current V_{reset} = +0.4V V_{reset} = 0V		 0.1 0.4	 0.4 1.5	mA
V_{OL}	Low Level Output Voltage V_{CC} = +15V, $I_{O(sink)}$ = 10mA $I_{O(sink)}$ = 50mA $I_{O(sink)}$ = 100mA $I_{O(sink)}$ = 200mA V_{CC} = +5V, $I_{O(sink)}$ = 8mA $I_{O(sink)}$ = 5mA		 0.1 0.4 2 2.5 0.3 0.25	 0.25 0.75 2.5 0.4 0.35	V
V_{OH}	High Level Output Voltage V_{CC} = +15V, $I_{O(source)}$ = 200mA $I_{O(source)}$ = 100mA V_{CC} = +5V, $I_{O(source)}$ = 100mA	 12.75 2.75	 12.5 13.3 3.3		V
$I_{dis(off)}$	Discharge Pin Leakage Curren (output high) (V_{dis} = 10V)		20	100	nA
$V_{dis(sat)}$	Discharge pin Saturation Voltage (output low) - (note 4) V_{CC} = +15V, I_{dis} = 15mA V_{CC} = +5V, I_{dis} = 4.5mA		 180 80	 480 200	mV
t_r t_f	Output Rise Time Output Fall Time		100 100	300 300	ns
toff	Turn off Time - (note 5) (Vreset = V_{CC})		0.5		µs

Notes : 1. Supply current when output is high is typically 1mA less.
2. Tested at VCC = +5V and VCC = +15V.
3. This will determine the maximum value of RA + RB for +15V operation the max total is R = 20MΩ and for 5V operation the max total R = 3.5MΩ.
is necessary, providing the package dissipation rating will not be exceeded.
5. Time mesaured from a positive going input pulse from 0 to 0.8x VCC into the threshold to the drop from high to low of theoutput trigger is tied to threshold

Figure 1 : Minimum Pulse Width Required for Supply Voltage

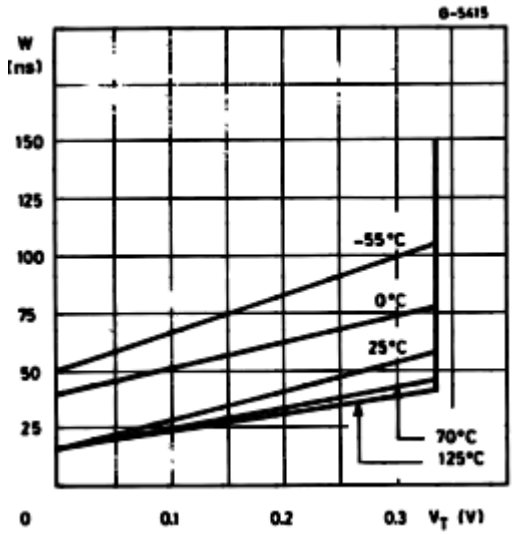


Figure 2 : Supply Current versus Trigering

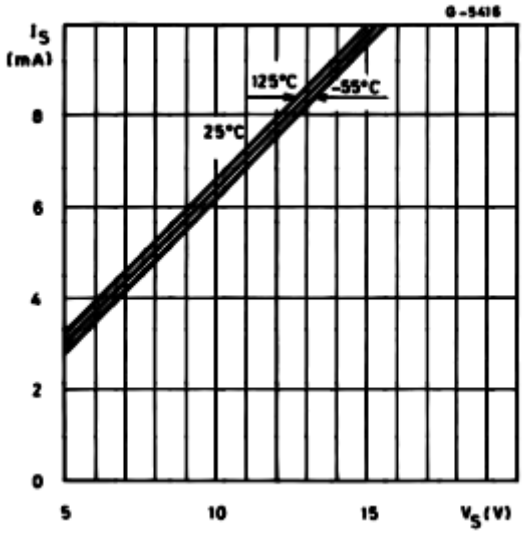


Figure 3 : Delay Time versus Temperature

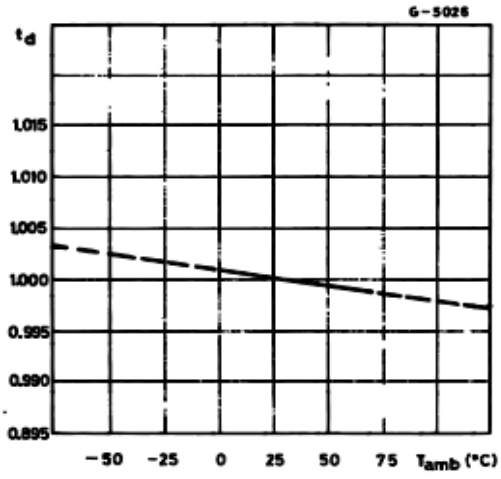


Figure 4 : Low Output Voltage versus Output Sink Current

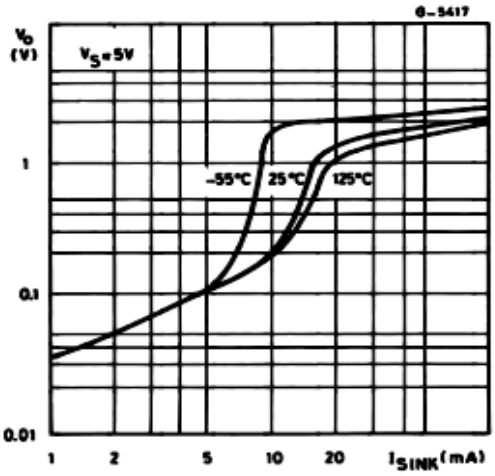


Figure 5 : Low Output Voltage versus Output Sink Current

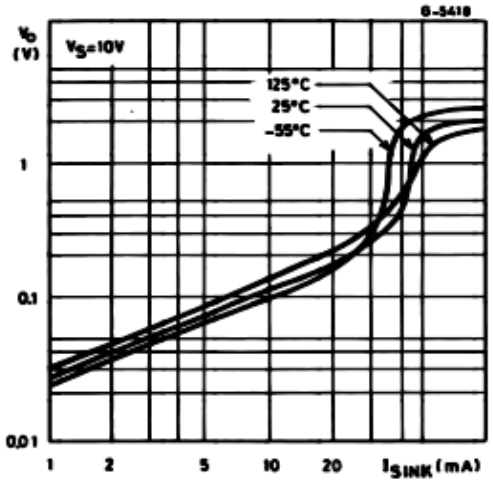


Figure 6 : Low Output Voltage versus Output Sink Current

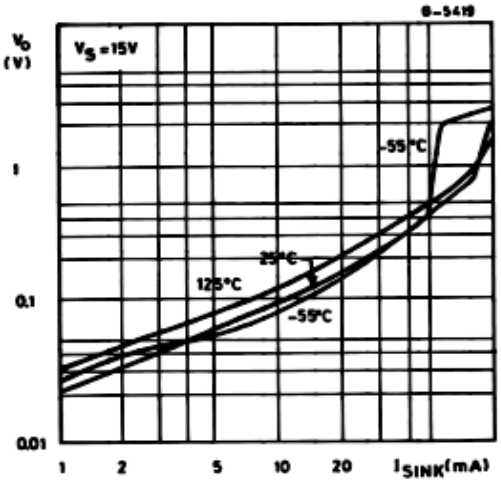


Figure 7 : High Output Voltage Drop versus Output

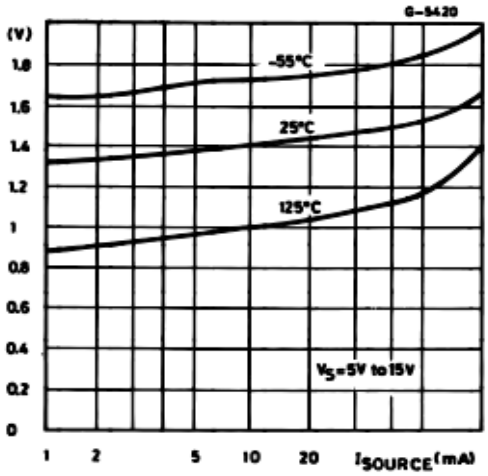


Figure 8 : Delay Time versus Supply Voltage

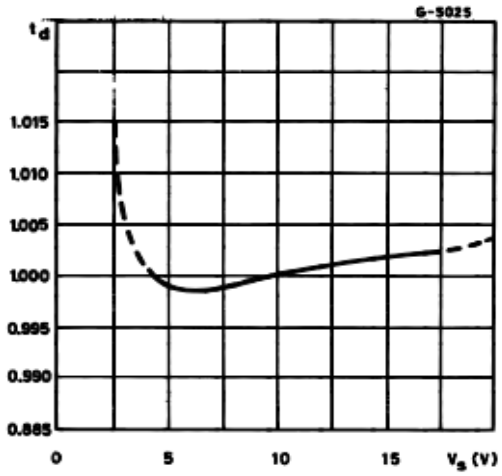
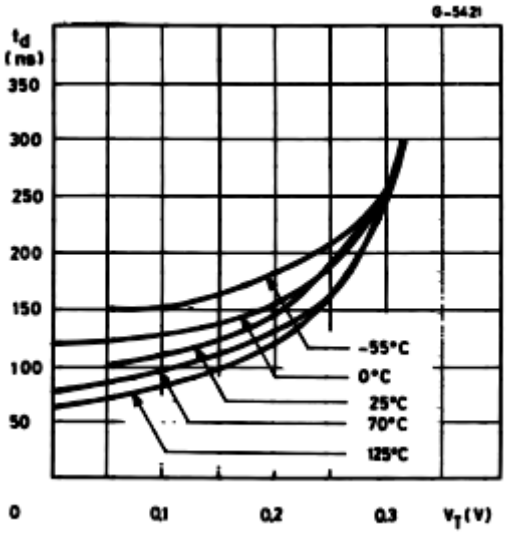


Figure 9 : Propagation Delay versus Voltage Level of Trigger Value

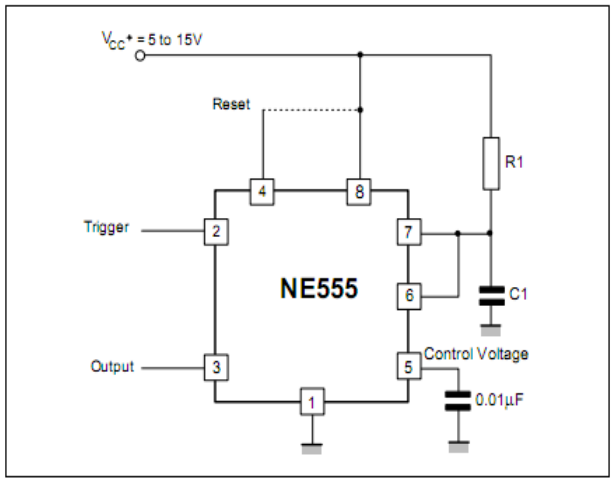


APPLICATION INFORMATION

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to figure 10 the external capaci-tor is initially held discharged by a transistor inside the timer.

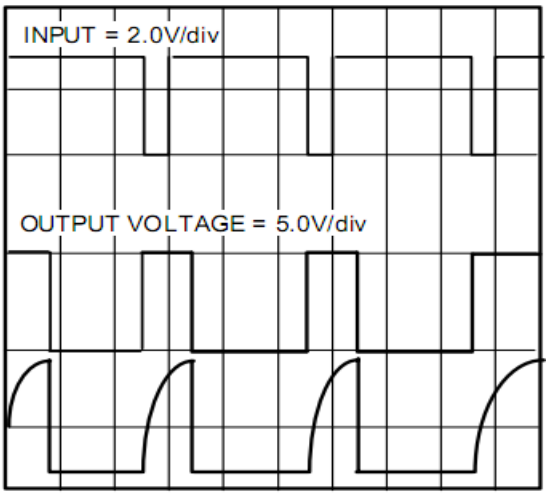
Figure 10



The circuit triggers on a negative-going input signal when the level reaches 1/3 Vcc. Once triggered, thecircuit remains in this state until the set time has elapsed, even if it is triggered again during this in-terval. The duration of the output HIGH state is given by t = 1.1 R1C1 and is easily determined by figure 12.Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the exter- nal capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse in ap- plied, the output is driven to its LOW state. When a negative trigger pulse is applied to pin 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant τ = R1C1. When the volt- age across the capacitor equals 2/3 Vcc, the comparator resets the flip-flop which then discharge the capacitor rapidly and drivers the output to its LOW state. Figure 11 shows the actual waveforms generated in this mode of operation.When Reset is not used, it should be tied high to avoid any possibly or false triggering.

Figure 11

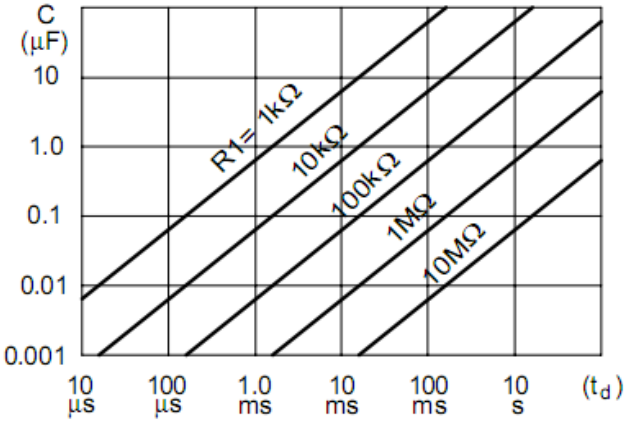
t = 0.1 ms / div



CAPACITOR VOLTAGE = 2.0V/div

R1 = 9.1kΩ, C1 = 0.01µF, R_L = 1kΩ

Figure 12



ASTABLE OPERATION

When the circuit is connected as shown in figure 13 (pin 2 and 6 connected) it riggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only.Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 Vcc and 2/3 Vcc. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 13

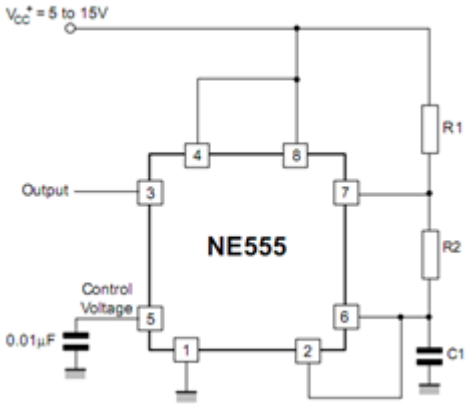


Figure 14 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by :

$t_1 = 0.693 (R_1 + R_2) C_1$

and the discharge time (output LOW) by :

$t_2 = 0.693 (R_2) C_1$

Thus the total period T is given by :

$T = t_1 + t_2 = 0.693 (R_1 + 2_{R2}) C_1$

The frequency ofoscillation is them :

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2)\, C_1}$$

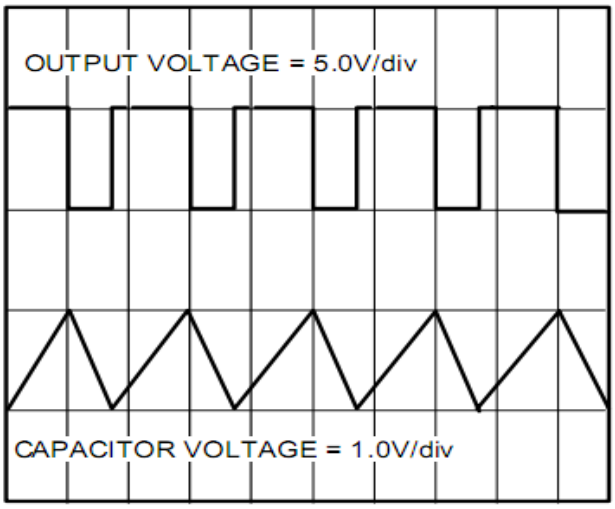
and may be easily found by figure 15.

The duty cycle is given by :

$$D = \frac{R_2}{R_1 + 2R_2}$$

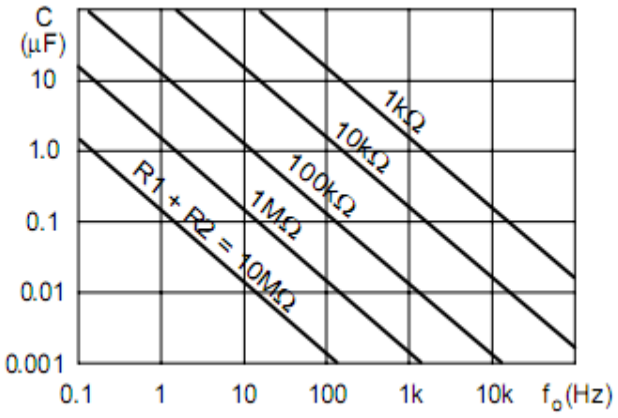
Figure 14

t = 0.5 ms / div



R1 = R2 = 4.8kΩ, C1= 0.1µF, R_L= 1kΩ

Figure 15 : Free Running Frequency versus R1,R2 and C1



PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train,the output pulse width can be modulated by a signal applied to pin 5. Figure 16 shows the circuit.

Figure 16 : Pulse Width

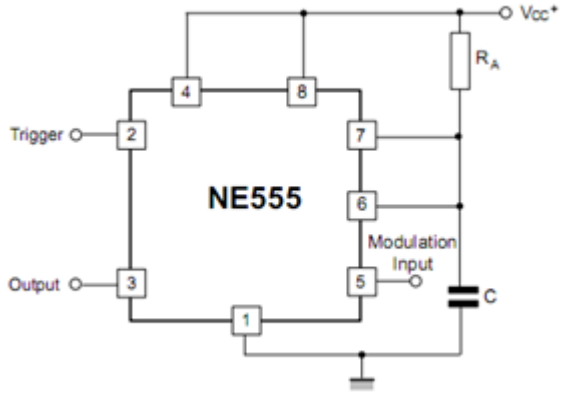


Figure 17.

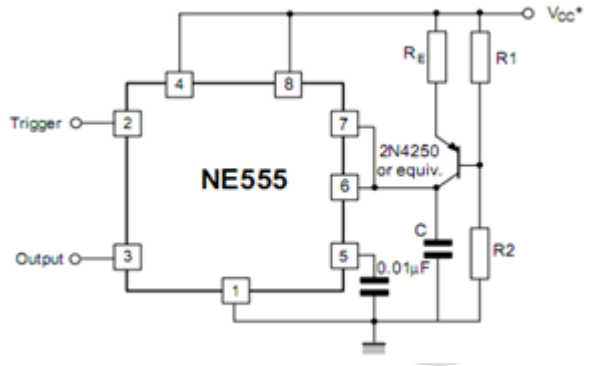
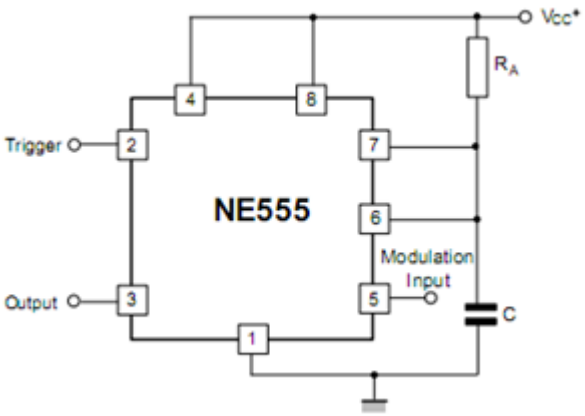


Figure 18 shows waveforms generator by the linear ramp.

The time interval is given by :

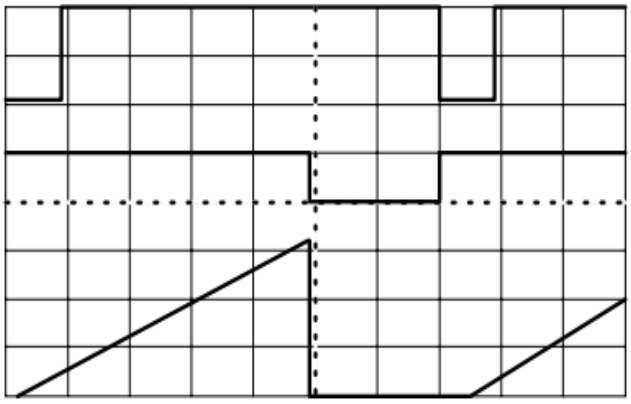
$$T = \frac{(2/3\ V_{CC}\ R_E\ (R_{1+}\ R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_{1+}\ R_2)} \quad V_{BE} = 0.6V$$

Figure 18 : Linear Ramp.



LINEAR RAMP

When the pullup resistor, RA, in the monostable cir-cuit is replaced by a constant current source, a linear ramp is generated. Figure 17 shows a circuit con-figuration that will perform this function.



V_{CC} = 5V Top trace : input 3V/DIV
Time = 20μs/DIV Middle trace : output 5V/DIV
R_1 = 47kΩ Bottom trace : output 5V/DIV
R_2 = 100kΩ Bottom trace : capacitor voltage
R_E = 2.7kΩ 1V/DIV
C = 0.01μF

50% DUTY CYCLE OSCILLATOR

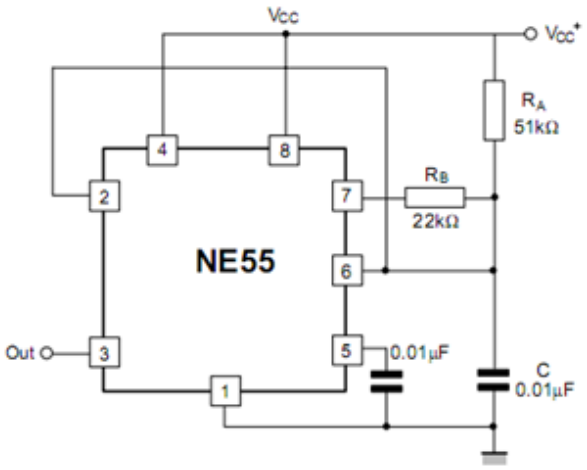
For a 50% duty cycle the resistors RA and RE may be connected as in figure 19. The time preriod for the output high is the same as previous,t1 = 0.693 RA C.
For the output low it is 2 =

$$[(R_A R_B)/(R_A + R_B)]\ C \ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

Figure 19 : 50% Duty Cycle Oscillator



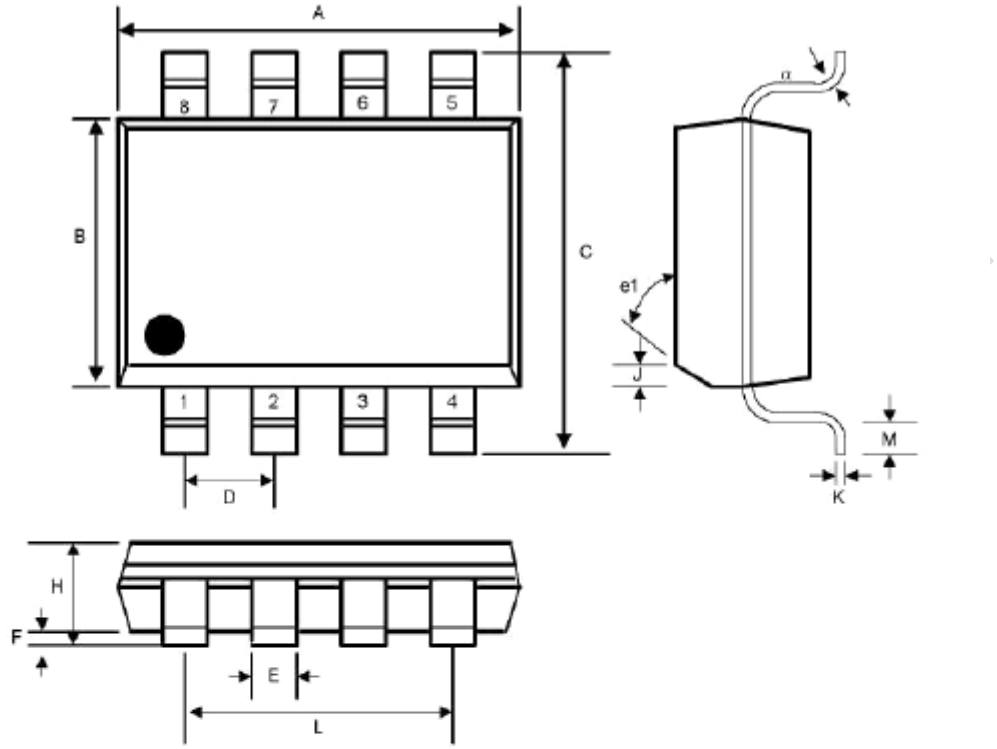
than 1/2 RA because the junction of RA and RB can-not bring pin 2 down to 1/3 VCC and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic

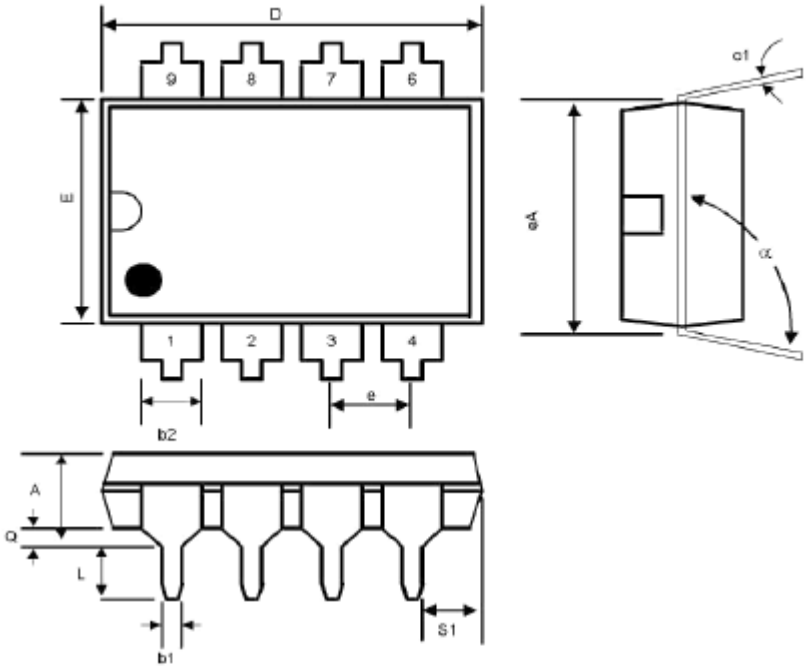
PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.188	0.197	4.80	5.00	-
B	0.149	0.158	3.80	4.00	-
C	0.228	0.244	5.80	6.20	-
D	0.050 BSC		1.27 BSC		-
E	0.013	0.020	0.33	0.51	-
F	0.004	0.010	0.10	0.25	-
H	0.053	0.069	1.35	1.75	-
J	0.011	0.019	0.28	0.48	
K	0.007	0.010	0.19	0.25	-
M	0.016	0.050	0.40	1.27	
L	0.150 REF		3.81 REF		-
e1	45^0		45^0		-
α	0^0	8^0	0^0	8^0	-

DIP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b1	0.014	0.023	0.36	0.58	-
b2	0.045	0.065	1.14	1.65	-
c1	0.008	0.015	0.20	0.38	-
D	0.355	0.400	9.02	10.16	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	-
s1	0.005	-	0.13	-	-
α	90^0	105^0	90^0	105^0	-