TOP ONE SEMI CONDUCTOR

OP07

Ultralow Offset Voltage t Operational Amplifiers

GENERAL DESCRIPTION

The OP07 has very low input offset voltage (75 μV max for OP07E) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external null-ing. The OP07 also features low input bias current (± 4 nA for OP07E) and high open-loop gain (200 V/mV for OP07E). The low offsets and high open-loop gain make the OP07 particularly useful for high-gain instrumentation applications.

The wide input voltage range of ± 13 V minimum combined with high CMRR of 106 dB (OP07E) and high input impedace pro-vides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or Variations in temperature is excellent. The Accuracy and stability of the OP07, even at high Gain, combined with the freedom from external Nulling have made the OP07 an industry Standard for instrumentation applications. The OP07 is available in two standard performance Grades. The OP07E is specified for operation Over the 0°C to 70°C range, and OP07C over The –40°C to +85°C temperature range. The OP07 is available in epoxy 8-lead Mini-DIP and 8-lead SOIC. It is a direct replacement for 725,108A, and OP05 amplifiers; 741-types may Be directly replaced by removing the 741's Nulling potentiometer. For improved Specifications, see the OP177 or OP1177. For Ceramic DIP and TO-99 packages and standard Micro circuit (SMD) versions, see the OP77.

FEATURES

- Low VOS: 75μV Max
- Low VOS Drift: 1.3μV /℃ Max
- Ultra-Stable vs. Time: 1.5μV /Month Max
- Low Noise: 0.6μV p-p Max
- Wide Input Voltage Range: ±14 V
- Wide Supply Voltage Range: 3 V to 18 V
- Fits 725,108A/308A, 741, AD510 Sockets

125℃ Temperature-Tested Dice

APPLICATIONS

- Wireless Base Station Control Circuits
- Optical Network Control Circuits
- Instrumentation
- Sensors and Controls
- Thermocouples
- RTDs
- Strain Bridges
- Shunt Current Measurements Precision Filters

FUNCTIONAL DIAGRAM

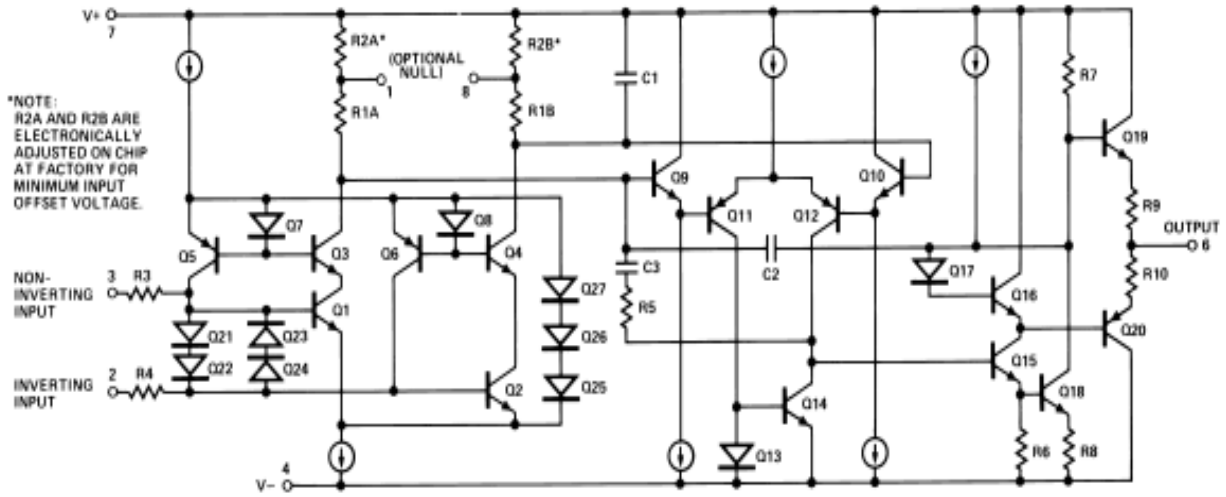


Figure 1. Simplified Schematic

REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

OP07–SPECIFICATIONS

OP07E ELECTRICAL CHARACTERISTICS (VS = ⎣15 V, TA = 25⎤ C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	VOS			30	75	μV
Long-Term Vos Stability	Vos/Time			0.3	1.5	μV/Mo
Input offset Current	Ios			0.5	3.8	nA
Input Bias Current	IB			±1.2	± 4.0	nA
Input Noise Voltage	en p-p	0.1 Hz to 10 Hz[3]		0.35	0.6	μV P-P
Input Noise Voltage Density	en	f_O = 10 Hz		10.3	18.0	nV$\sqrt{HZ}$
		f_O = 100 Hz[3]		10.0	13.0	nV$\sqrt{HZ}$
		f_O = 1K Hz		9.6	11.0	nV$\sqrt{HZ}$
Input Noise Current	In p-p			14	30	pA p-p
Input Noise Current Density	In	f_O = 10 Hz		0.32	0.80	pA$\sqrt{HZ}$

		f_O = 100 Hz[3]		0.14	0.23	pA $\sqrt{HZ}$
		f_O = 1K Hz		0.12	0.17	pA $\sqrt{HZ}$
Input resistance-Differential Mode4	R_{IN}		15	50		mΩ
Input Resistance—Common-Mode	R_{INCM}			160		GΩ
Input Voltage Range	IVR		±13	±14		V
Common-Mode Rejection Ratio	CMRR	VCM = ± 13 V	106	123		dB
Power Supply Rejection Ratio	PSRR	VS = ± 3 V to ± 18 V		5	20	μV/V
Large-Signal Voltage Gain	AVO	RL ≥ 2 kΩ, VO = ± 10 V	200	500		V/mV
		RL ≥ 500 Ω, VO = ± 0.5 V,				
		VS = ± 3 V[4]	150	400		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	Vo	RL ≥ 10 kΩ	±12.5	±13.0		V
		RL ≥ 2 kΩ	±12.0	±12.8		V
		RL ≥ 1 kΩ	±10.5	±12.0		V
DYNAMIC PERFORMANCE						
Slew Rate	SR	RL ≥ 2 kΩ[3]	0.1	0.3		V/μs
Closed-Loop Bandwidth	BW	AVOL = 1[5]	0.4	0.6		MHz
Closed-Loop Output Resistance	Ro	Vo = 0, Io = 0		60		Ω
Power Consumption	Pd	Vs = ± 15 V, No Load		75	120	mW
Offset Adjustment Range		Rp = 20 kΩ		± 4		mV

NOTES

1、Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

2、Long-term input offset voltage stability refers to the averaged trend time of VOS vs. Time over extended periods after the first 30 days of operation. Excluding the ini-tial hour of operation, changes in VOS during the first 30 operating days are typically 2.5 μV refer to the typical performance curves. Parameter is sample tested.

3、Sample tested.

4、Guaranteed by design.

5、Guaranteed but not tested.

Specifications subject to change without notice.

OP07–SPECIFICATIONS

OP07E ELECTRICAL CHARACTERISTICS (VS = ±15 V, 0℃ ≤ TA ≤ 70℃, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage[1]	Vos			45	130	μV
Voltage Drift without External Trim[2]	TCVos			0.3	1.3	μV/°C
Voltage Drift with External Trim[3]	TCVosN	Rp=20kΩ		0.3	1.3	μV/°C
Input Offset Current	I_{OS}			0.9	5.3	nA
Input Offset Current Drift	TCIos			8	35	μV/°C
Input Bias Current	IB			±1.5	±1.5	nA
Input Bias Current Drift	TCI_B			13	35	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ± 13 V	103	123		dB
Power Supply Rejection Ratio	PSRR	Vs= ± 13 V to ± 18 V		7	32	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ± 10 V	180	450		V/mV
OUTPUT CHARACTERISTICS Output Voltage Swing	Vo	R_L≥ 10 kΩ	±12 V	±12 .6V		V

NOTES

1、Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

2、Guaranteed by design.

3、Sample tested.

Specifications subject to change without notice.

OP07C ELECTRICAL CHARACTERISTICS(VS = ±15 V, -40℃ ≤ TA ≤ −85℃, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage[1]	Vos			85	250	μV
Voltage Drift without External Trim[2]	TCVos			0.5	1.8	μV/°C
Voltage Drift with External Trim[3]	TCVosN	Rp=20kΩ		0.4	1.8	μV/°C
Input Offset Current	I_{OS}			1.6	8.0	nA
Input Offset Current Drift	TCIos			12	50	μV/°C
Input Bias Current	IB			±2.2	±9.0	nA
Input Bias Current Drift	TCI_B			18	50	pA/°C
Input Voltage Range	IVR		±13	±13.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ± 13 V	97	120		dB
Power Supply Rejection Ratio	PSRR	Vs= ± 13 V to ± 18 V		10	51	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ± 10 V	100	400		V/mV
OUTPUT CHARACTERISTICS Output Voltage Swing	Vo	R_L≥ 10 kΩ	±11	±12 .6V		V

NOTES

1、Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

2、Guaranteed by design.

3、Sample tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (VS) . . . . . ± 22 V
Input Voltage* . . . . . ± 22 V
Differential Input Voltage . . . . . ± 30 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
S, P Packages . . . . . –65°C to +125°C
Operating Temperature Range
OP07E . . . . . 0°C to 70°C
OP07C . . . . . –40°C to +85°C
Junction Temperature Range . . . . . 150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
*For supply voltages less than ± 22 V, the absolute maximum input voltage is equalto the supply voltage.

Package Type	θ_{JA} *	θ_{JC}	Units
8-Lead Plastic DIP (P)	103	43	℃/W
8-Lead SOIC (S)	158	43	℃/W

* θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package, θ_{JA} is specified for device soldered to printed circuit board for SO package.

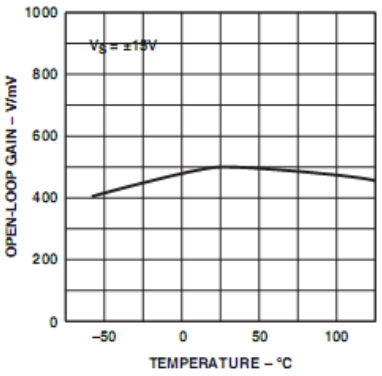
ORDERING GUIDE

Model	Temperature Range	Package Description	Package option	Branding Information
OP07EP	0°C to 70°C	8-Lead Epoxy DIP	P-8	
OP07CP	－40°C to 85°C	8-Lead Epoxy DIP	P-8	
OP07CS	－40°C to 85°C	8-Lead SOIC	S-8	

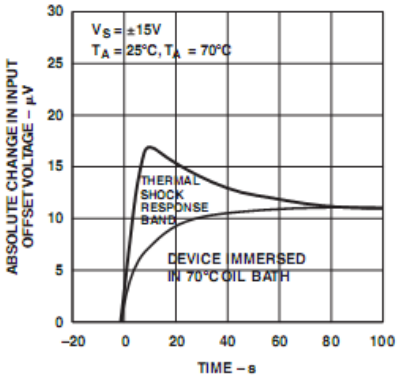
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP07 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recom-mended to avoid performance degradation or loss of functionality.

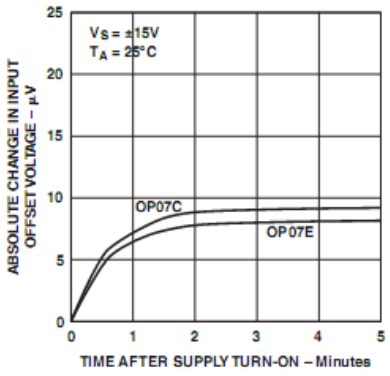
OP07 – Typical Performance Characteristics



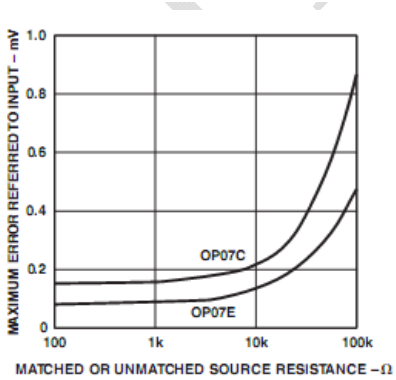
TPC 1. Open-Loop Gain vs. Temperature



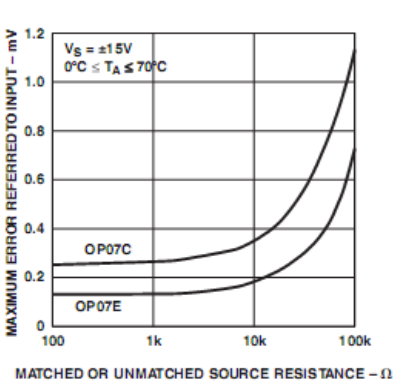
TPC 2. Offset Voltage Change Due to Thermal Shock



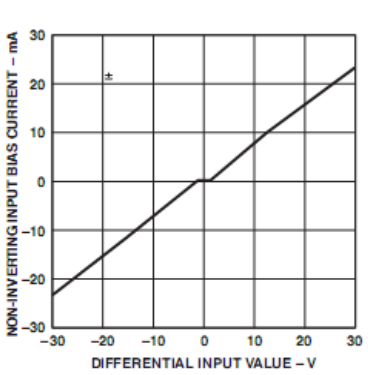
TPC 3. Warm-Up Drift



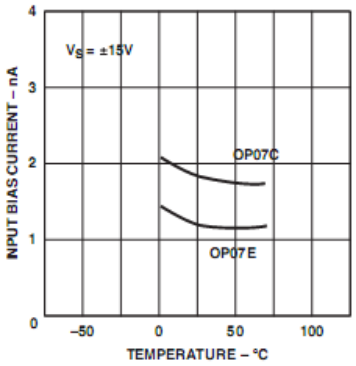
TPC 4. Maximum Error vs. Source Resistance



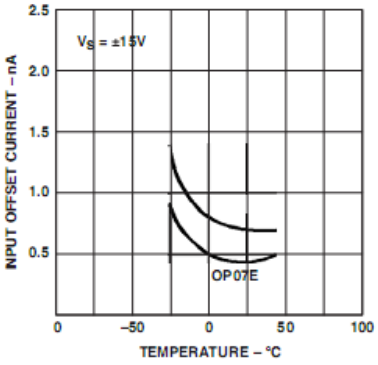
TPC 5. Maximum Error vs. Source Resistance



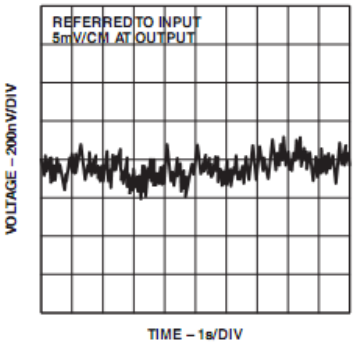
TPC 6. Input Bias Current vs. Differential Input Voltage



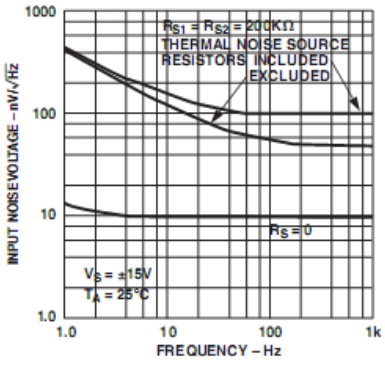
TPC 7. Input Bias Current vs. Temperature



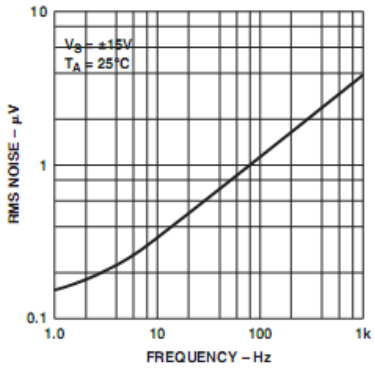
TPC 8. Input Offset Current vs. Temperature



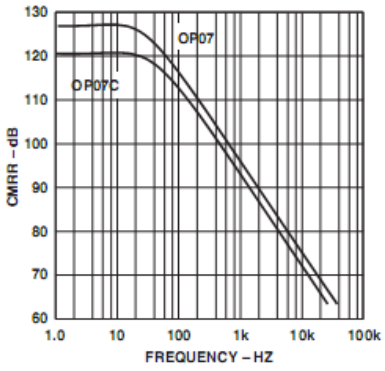
TPC 9. Low Frequency Noise



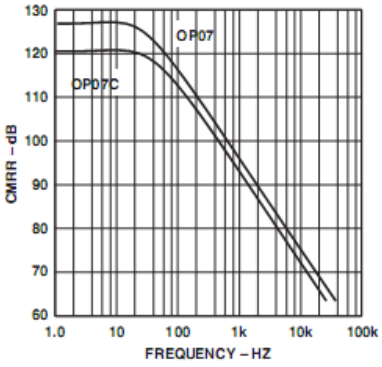
TPC 10. Total Input Noise Voltage vs. Frequency



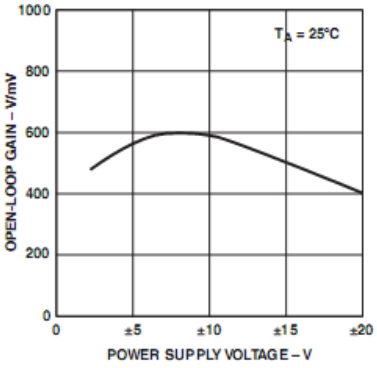
TPC 11. Input Wideband Noise vs Bandwidth (0.1 Hz to Frequency Indicated)



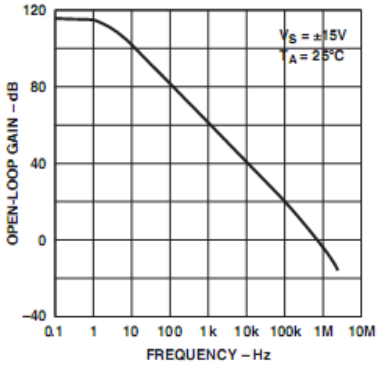
TPC 12. CMRR vs. Frequency



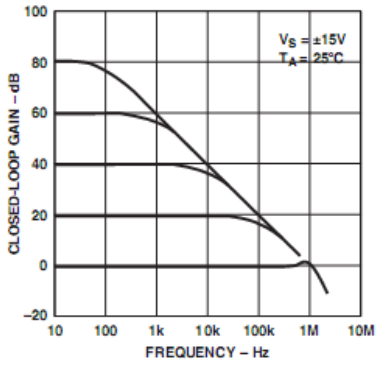
TPC 13. PSRR vs. Frequency



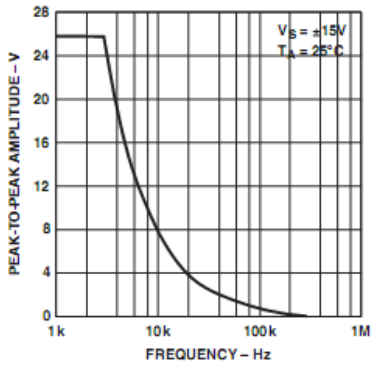
TPC 14. Open-Loop Gain vs Power Supply Voltage



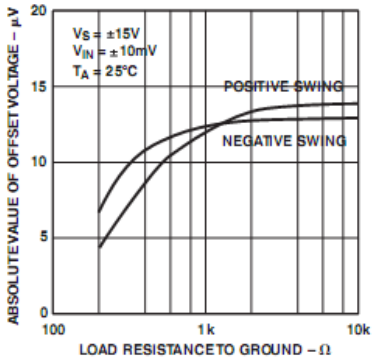
TPC 15. Open-Loop Frequency Response



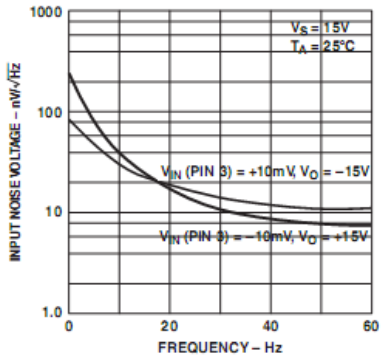
TPC 16. Closed-Loop Response for Various Gain Configurations



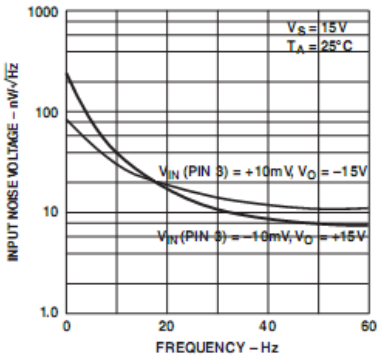
TPC 17. Maximum Output Swing vs. Frequency



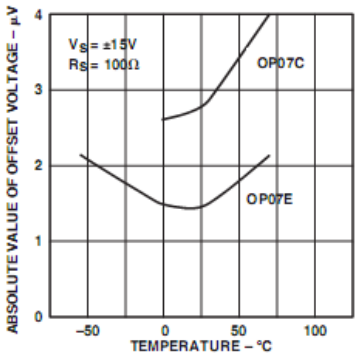
TPC 18. Maximum Output Voltage vs. Load Resistance



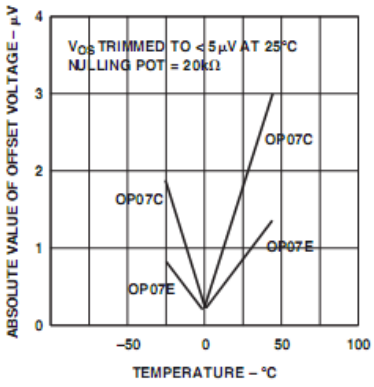
TPC 19. Power Consumption vs. Power Supply



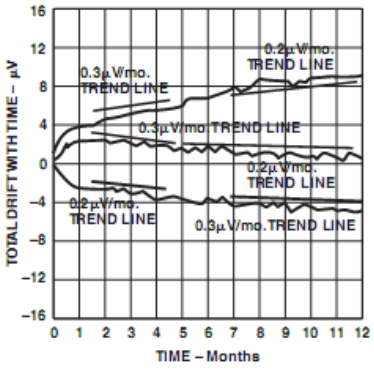
TPC 20. Output Short-Circuit Current vs. Time



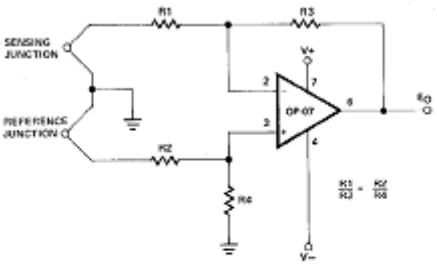
TPC 21. Untrimmed Offset Voltage vs. Temperature



TPC 22. Trimmed Offset Voltage vs. Temperature



TPC 23. Offset Voltage Stability vs. Time



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 8. High-Stability Thermocouple Amplifier

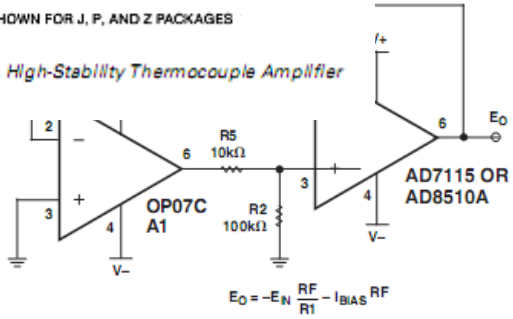
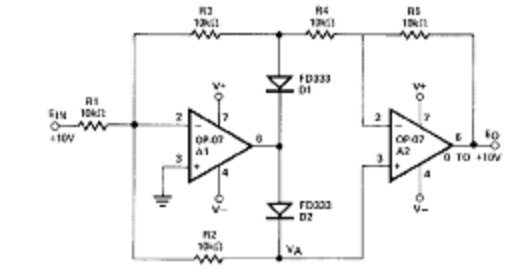


Figure 2. Typical Offset Voltage Test Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 9. Precision Absolute-Value Circuit

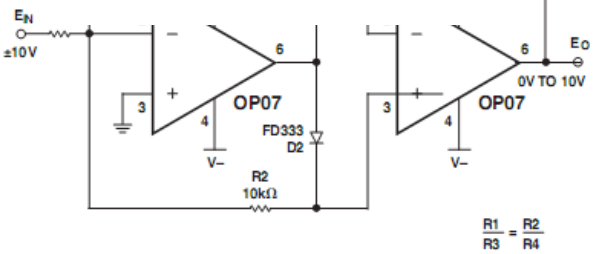


Figure 5. Burn-In circuit

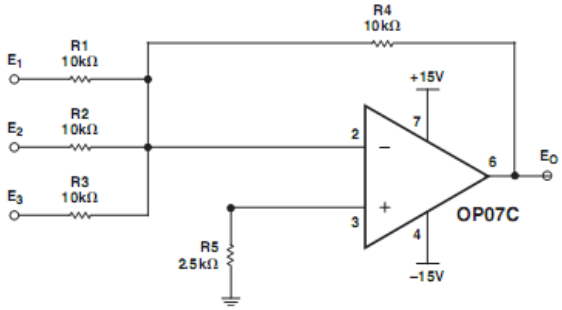
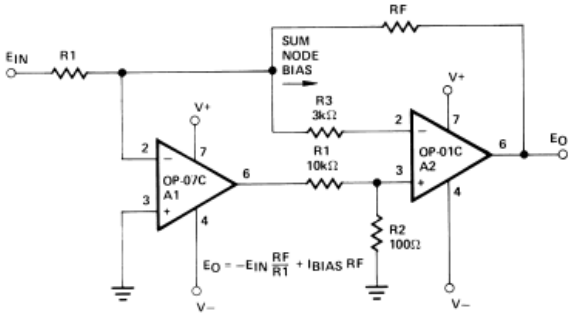


Figure 3. Typical Low-Frequency Noise Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 6. High-Speed, Low VOS Composite Amplifier

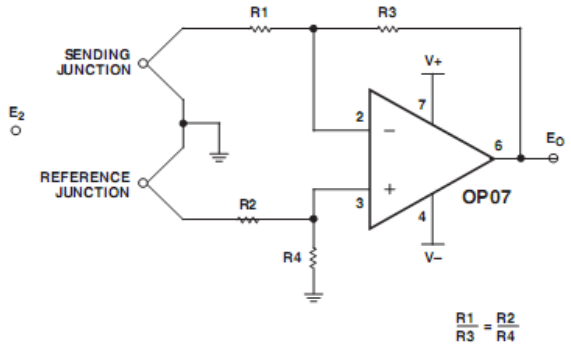
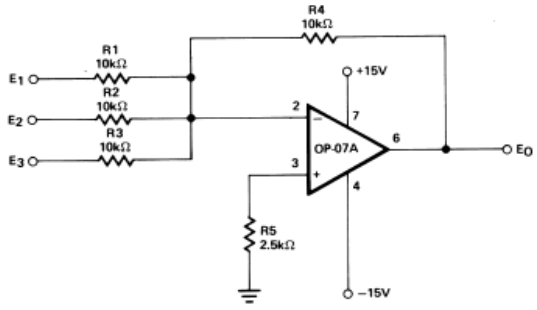


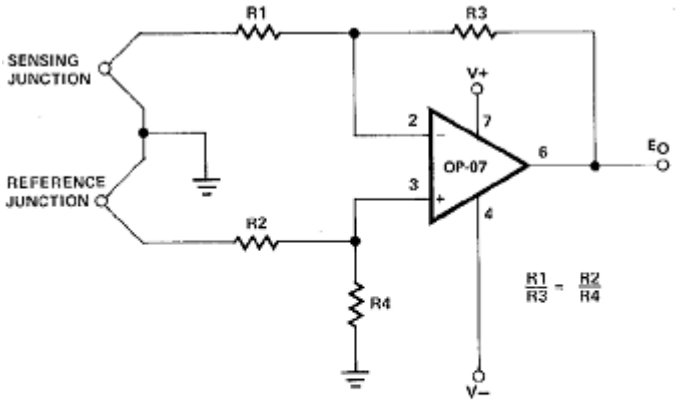
Figure 4. Optional Offset Nulling Circuit



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

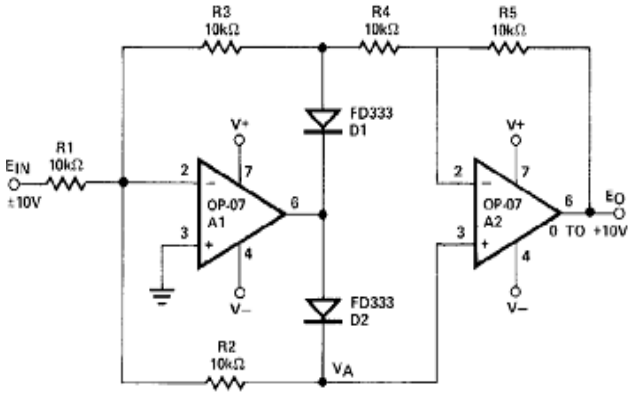
Figure 7. Adjustment-Free Precision Summing Amplifier

TYPICAL APPLICATIONS



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

Figure 8. High-Stability Thermocouple Amplifier



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

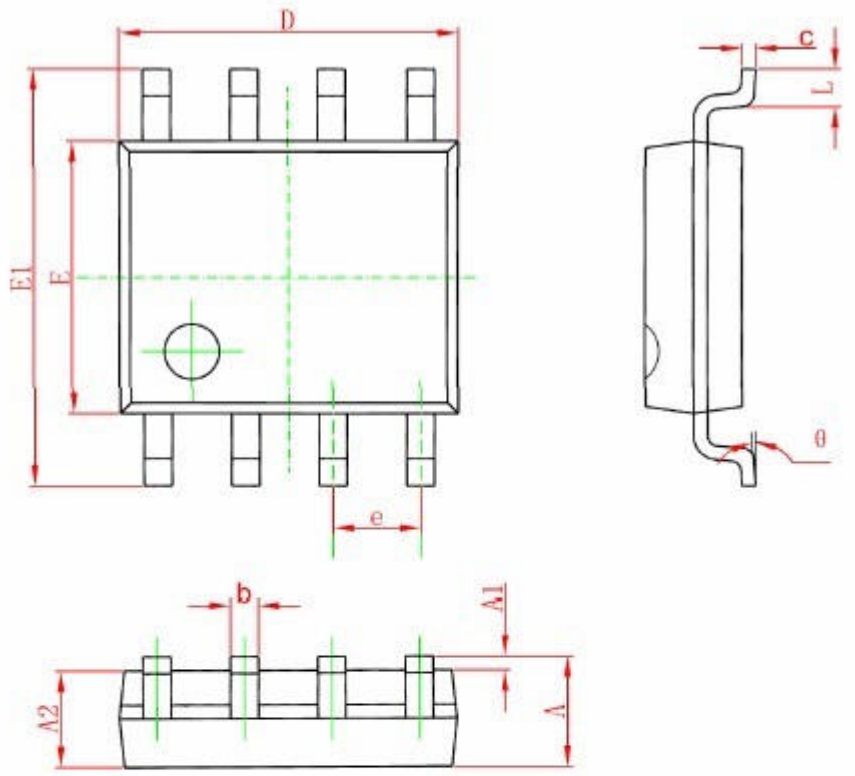
Figure 9. Precision Absolute-Value Circuit

APPLICATIONS INFORMATION

OP07 series units may be substituted directly into 725, 108A/ 308A* and OP05 sockets with or without removal of external compensation or nulling components. Additionally, the OP07 may be used in unnulled 741 type sockets. However, if conven-tional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP07 operation. OP07 offset voltage may be nulled to zero through use of a potentiometer (see offset nulling circuit diagram). PRECISION ABSOLUTE-VALUE CIRCUIT The OP07 Provides stable operation with load capacitance Of up to 500 pF and ± 10 V swings; larger Capacitances should be decoupled with a 50 Q Decoupling resistor. Stray thermoelectric Voltages generated by dissimilar metals at the Contacts to the input terminals can degrade drift Performance. Therefore, best operation will be Obtained when both input con-tacts are Maintained at the same temperature, preferably Close to the package temperature.

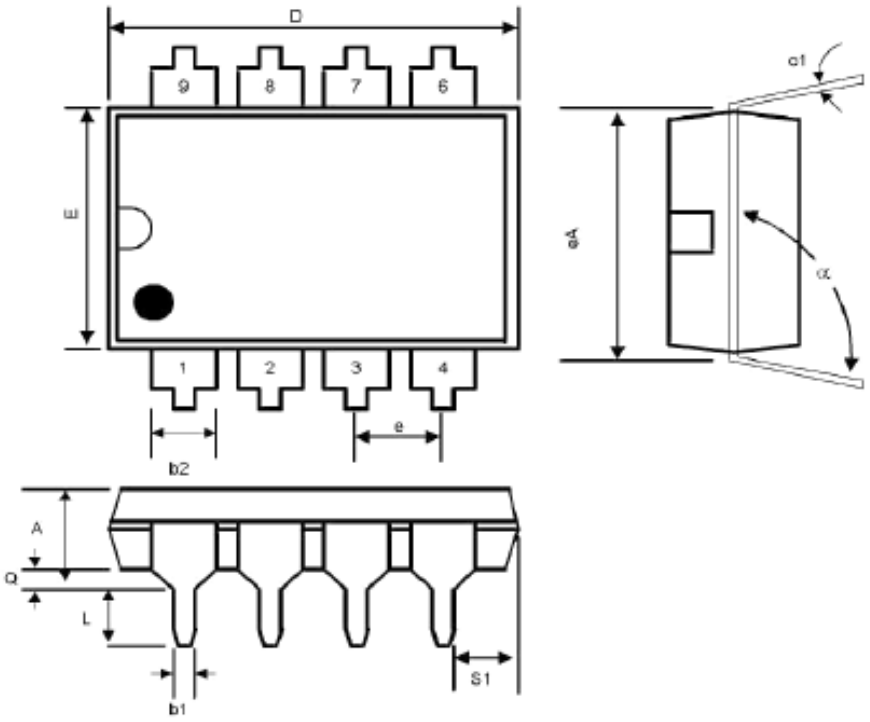
PACKAGE DESCRIPTION

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b1	0.014	0.023	0.36	0.58	-
b2	0.045	0.065	1.14	1.65	-
c1	0.008	0.015	0.20	0.38	-
D	0.355	0.400	9.02	10.16	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	-
s1	0.005	-	0.13	-	-
α	90^0	105^0	90^0	105^0	-